AMENDMENTS TO THE CLAIMS

Claims 1-49 have been allowed in the instant application. Claims 33, 44, and 45 have been amended. Claim 43 has been cancelled. The Applicant requests reconsideration of the claims in view of the following amendments reflected in the listing of claims.

Listing of claims:

1. (Previously Presented) A method for processing television signals, the method comprising:

receiving, over the air, an inband signal by a single chip integrated DTV receiver;

demodulating said received inband signal within said single chip DTV receiver;

receiving, over the air, an out-of-band signal corresponding to said received inband signal by said single chip integrated DTV receiver; and

processing said received out-of-band signal within said single chip integrated DTV receiver.

2. (Previously Presented) The method according to claim 1, wherein said received inband signal is one or more of a VSB signal, a NTSC signal, and a QAM signal.

3. (Previously Presented) The method according to claim 1, comprising:

if said received inband signal is a VSB signal, error correcting said demodulated received inband signal within said single chip integrated DTV receiver to generate an error corrected ATSC compliant signal; and

if said received inband signal is a QAM signal, error correcting said demodulated received inband signal within said single chip integrated DTV receiver to generate an error corrected ITU-T J.83 compliant signal.

4. (Previously Presented) The method according to claim 3, wherein said ITU-T J.83 compliant signal is compliant with one or more of Annex A, Annex B, and Annex C of ITU-T J.83.

5. (Previously Presented) The method according to claim 3, comprising:

if said received inband signal is a VSB signal, equalizing said error corrected ATSC signal within said single chip integrated DTV receiver; and

if said received inband signal is a QAM signal, equalizing said error corrected ITU-T J.83 compliant signal within said single chip integrated DTV receiver.

6. (Previously Presented) The method according to claim 1, comprising generating from within said single chip integrated DTV receiver, an output MPEG transport stream from said demodulated received inband signal.

7. (Original) The method according to clam 6, wherein said output MPEG transport stream is a serial MPEG transport stream or a parallel MPEG transport stream.

8. (Previously Presented) The method according to claim 1, comprising decoding said demodulated received inband signal within said single chip integrated DTV receiver, if said received inband signal is an NTSC signal.

9. (Previously Presented) The method according to claim 8, comprising generating from within said single chip integrated DTV receiver, one or more of an I^2S audio output, a stereo audio output, a monaural audio output, and a

multiplexed baseband audio output from said decoded demodulated received inband signal.

10. (Previously Presented) The method according to claim 1, comprising generating a composite NTSC signal from said demodulated received signal within said single chip integrated DTV receiver, if said received signal is an NTSC signal.

11. (Previously Presented) The method according to claim 1, comprising demodulating said received out-of-band signal within said single chip integrated DTV receiver.

12. (Previously Presented) The method according to claim 11, comprising demodulating said received out-of-band signal within said single chip integrated DTV receiver utilizing a QPSK demodulator.

13. (Previously Presented) The method according to claim 11, comprising error correcting said demodulated received out-of-band signal within said single chip integrated DTV receiver.

14. (Previously Presented) The method according to claim 1, comprising generating an output out-of-band transport stream from said processed received out-of-band signal from within said single chip integrated DTV receiver.

15. (Original) The method according to claim 14, wherein said out-of-band transport stream comprises CableCard encryption and security data.

16. (Previously Presented) The method according to claim 1, comprising controlling said demodulating of said received inband signal via an on-chip processor integrated within said single chip integrated DTV receiver.

17. (Previously Presented) A machine-readable storage having stored thereon, a computer program having at least one code section for processing television signals, the at least one code section being executable by a machine for causing the machine to perform steps comprising:

receiving, over the air, an inband signal by a single chip integrated DTV receiver;

demodulating said received inband signal within said single chip DTV receiver;

receiving, over the air, an out-of-band signal corresponding to said received signal by said single chip integrated DTV receiver; and

processing said received out-of-band signal within said single chip integrated DTV receiver.

18. (Previously Presented) The machine-readable storage according to claim 17, wherein said received signal is one or more of a VSB signal, a NTSC signal, and a QAM signal.

19. (Previously Presented) The machine-readable storage according to claim 17, comprising:

code for error correcting said demodulated received inband signal within said single chip integrated DTV receiver to generate an error corrected ATSC compliant signal, if said received inband signal is a VSB signal; and

code for error correcting said demodulated received inband signal within said single chip integrated DTV receiver to generate an error corrected ITU-T J.83 compliant signal, if said received inband signal is a QAM signal.

20. (Previously Presented) The machine-readable storage according to claim 19, wherein said ITU-T J.83 compliant signal is compliant with one or more of Annex A, Annex B, and Annex C of ITU-T J.83.

21. (Previously Presented) The machine-readable storage according to claim 19, comprising:

code for equalizing said error corrected ATSC signal within said single chip integrated DTV receiver, if said received inband signal is a VSB signal; and

code for equalizing said error corrected ITU-T J.83 compliant signal within said single chip integrated DTV receiver, if said received inband signal is a QAM signal.

22. (Previously Presented) The machine-readable storage according to claim 17, comprising code for generating from within said single chip integrated DTV receiver, an output MPEG transport stream from said demodulated received inband signal.

23. (Original) The machine-readable storage according to clam 22, wherein said output MPEG transport stream is a serial MPEG transport stream or a parallel MPEG transport stream.

24. (Previously Presented) The machine-readable storage according to claim 17, comprising code for decoding said demodulated received signal within said single chip integrated DTV receiver, if said received inband signal is an NTSC signal.

25. (Previously Presented) The machine-readable storage according to claim 24, comprising code for generating from within said single chip integrated DTV receiver, one or more of an I^2S audio output, a stereo audio output, a monaural audio output, and a multiplexed baseband audio output from said decoded demodulated received inband signal.

26. (Previously Presented) The machine-readable storage according to claim 17, comprising code for generating a composite NTSC signal from said demodulated received signal within said single chip integrated DTV receiver, if said received inband signal is an NTSC signal.

27. (Previously Presented) The machine-readable storage according to claim 17, comprising code for demodulating said received out-of-band signal within said single chip integrated DTV receiver.

28. (Previously Presented) The machine-readable storage according to claim 27, comprising code for demodulating said received out-of-band signal within said single chip integrated DTV receiver utilizing a QPSK demodulator.

29. (Previously Presented) The machine-readable storage according to claim 27, comprising code for error correcting said demodulated received out-of-band signal within said single chip integrated DTV receiver.

30. (Previously Presented) The machine-readable storage according to claim 17, comprising code for generating an output out-of-band transport stream from said processed received out-of-band signal from within said single chip integrated DTV receiver.

31. (Original) The machine-readable storage according to claim 30, wherein said out-of-band transport stream comprises CableCard encryption and security data.

32. (Previously Presented) The machine-readable storage according to claim 17, comprising code for controlling said demodulating of said received inband signal via an on-chip processor integrated within said single chip integrated DTV receiver.

33. (Currently Amended) A system for processing television signals, the system comprising:

an inband analog front end integrated in a single chip integrated DTV receiver that receives, over the air, an inband signal;

a first demodulator within said single chip DTV receiver that demodulates said received inband signal;

an out-of-band analog front end integrated in said single chip integrated DTV receiver that receives, over the air, an out-of-band signal corresponding to said received signal by; and

~~an out-of-band receiver~~ second demodulator ~~integrated~~ within said single chip integrated DTV receiver that ~~processes~~ demodulates said received out-of-band signal.

34. (Previously Presented) The system according to claim 33, wherein said received inband signal is one or more of a VSB signal, a NTSC signal, and a QAM signal.

35. (Previously Presented) The system according to claim 33, comprising:

an ATSC FEC that error corrects said demodulated received inband signal within said single chip integrated DTV receiver to generate an error corrected ATSC compliant signal, if said received inband signal is a VSB signal; and

and ITU-T J.83 compliant FEC that error corrects said demodulated received inband signal within said single chip integrated DTV receiver to generate an error corrected ITU-T J.83 compliant signal, if said received signal is a QAM signal.

36. (Previously Presented) The system according to claim 35, wherein said ITU-T J.83 compliant signal is compliant with one or more of Annex A, Annex B, and Annex C of ITU-T J.83.

37. (Previously Presented) The system according to claim 35, comprising:

at least one equalizer that equalizes said error corrected ATSC signal within said single chip integrated DTV receiver, if said received inband signal is a VSB signal; and

said at least one equalizer equalizes said error corrected ITU-T J.83 compliant signal within said single chip integrated DTV receiver, if said received inband signal is a QAM signal.

38. (Previously Presented) The system according to claim 33, comprising an inband output interface that generates from within said single chip integrated DTV receiver, an output MPEG transport stream from said demodulated received inband signal.

39. (Original) The system according to clam 38, wherein said output MPEG transport stream is a serial MPEG transport stream or a parallel MPEG transport stream.

40. (Previously Presented) The system according to claim 33, comprising a BTSC decoder that decodes said demodulated received inband signal within said single chip integrated DTV receiver, if said received inband signal is an NTSC signal.

41. (Previously Presented) The system according to claim 40, comprising one or both of said BTSC decoder and an audio DAC that generates from within said single chip integrated DTV receiver, one or more of an I^2S audio output, a stereo audio output, a monaural audio output, and a multiplexed baseband audio output from said decoded demodulated received inband signal.

42. (Previously Presented) The system according to claim 33, comprising a DAC that generates a composite NTSC signal from said demodulated received inband signal within said single chip integrated DTV receiver, if said received inband signal is an NTSC signal.

43. (Cancelled)

44. (Currently Amended) The system according to claim 33, ~~comprising a~~ wherein said second demodulator is a QPSK demodulator ~~that demodulates said received out-of-band signal within said single chip integrated DTV receiver~~.

45. (Currently Amended) The system according to claim [[43]]33, comprising one or both of a DVS-167 compliant FEC and a DVS-178 compliant FEC that error corrects said demodulated received out-of-band signal within said single chip integrated DTV receiver.

46. (Previously Presented) The system according to claim 33, comprising an out-of-band output interface that generates an output out-of-band transport stream from said processed received out-of-band signal from within said single chip integrated DTV receiver.

47. (Original) The system according to claim 46, wherein said out-of-band transport stream comprises CableCard encryption and security data.

48. (Previously Presented) The system according to claim 33, comprising an on-chip processor that controls said demodulating of said received inband signal within said single chip integrated DTV receiver.

49. (Previously Presented) The system according to claim 33, comprising a third overtone crystal which generates a 54 MHz clock signal which is coupled to said inband analog front end.